

## Kibra™ 480

### DDR3 and DDR4 Compliance Analyzer



PASSED  
PASSED  
PASSED  
PASSED  
PASSED  
PASSED  
PASSED  
PASSED  
PASSED  
PASSED  
FAILED  
Running...

[Timing Violation]

-----  
V04: Four ACT Window < tFAW (23 clocks)  
Violation occurred in Rank:1

Last First ACT command to here(ns) 0 000 000

Invalid ACT at 0.000 000 428 795 s

First ACT command at 0.000 000 412 560 s

ACT should have occurred after 0.000 000





## Key Features

- **Fast and easy compliance test**
  - ✓ Self-contained system offers easy connection and setup
  - ✓ Custom probe design supports higher speed modules
  - ✓ No calibration needed!
  - ✓ Free trace viewer runs on any PC
- **Comprehensive trigger and capture of JEDEC violations**
  - ✓ Detects over 65 JEDEC bus event and timing violations in real time
  - ✓ Interposers capture SPD data for fast configuration of the analyzer
- **Flexible, scalable platform**
  - ✓ Monitor two slots of quad rank DDR3 and DDR4 DIMMs concurrently
  - ✓ Supports registered and unbuffered DIMM types
  - ✓ Address multi-channel application by cascading analyzers

## DDR3 / DDR4 Bus & Timing Compliance

### Kibra 480 DDR4 Compliance Analyzer

The Teledyne LeCroy Kibra™ 480 is a stand-alone protocol compliance analyzer that provides comprehensive DDR3 and DDR4 JEDEC timing analysis. Based on the groundbreaking Kibra 480 Protocol Analyzer, the Kibra 480 Compliance Analyzer platform introduces a low cost compliance tool to non-intrusively monitor higher speed DDR3 as well as the new DDR4 specification without time consuming calibration and setup. The analyzer sits in line on a live system recording bus traffic while automatically identifying timing and protocol violations.

### Compliance Report

Upon detecting a compliance violation, the Kibra 480 displays any errors in an easy to understand report. The report notes the error, the violation type and the timing requirements that failed. A summary of violations is also displayed with an ability to hyperlink to any violation of interest.

### Easy Setup — No Calibration Needed!

Start using the Teledyne LeCroy Kibra 480 immediately without time consuming calibration. Simply enter the memory controller parameters and start recording. The software will automatically load JEDEC trigger values for the DIMM type and speed specified. Users can selectively disable or override any of the JEDEC triggers on-the-fly.

### Proprietary Probe Design for Higher Speed Memory

Teledyne LeCroy developed a custom ASIC for the Kibra 480 probe to support higher speed DDR modules. This proprietary probe implementation allows loss-less capture of DDR3 to 2133 MT/s; and DDR4 to speeds above 2400 MT/s. The probes are self-powered to provide instant signal lock—including reliable capture of the DDR4 power-on sequence. Separate probes are available for DDR3 and DDR4 supporting U-DIMM/R-DIMM as well as SO-DIMM form-factors.

## Probe Specifications

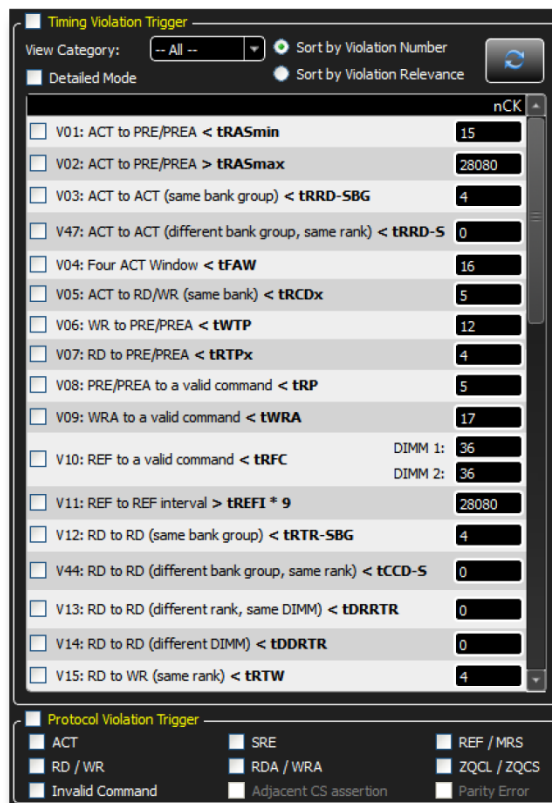
The Teledyne LeCroy Kibra 480 is available with several slot interposer probe options that provide the mechanical and electrical interface between the analyzer and the memory system-under-test. Probes are available capable of monitoring two slots of quad rank DIMMs or SO-DIMMs operating to 2400 MT/s. The probes operate non-intrusively and introduce less than 90 ps of latency to the DDR signal.

## CrossSync™ Support

CrossSync is the Teledyne LeCroy analyzer synchronization framework that enables time-aligned display of protocol traffic from multiple daisy-chained analyzers. By connecting the built-in sync ports on the Kibra 480, users can monitor multiple memory channels concurrently. The same interface can also be used to synchronize DDR4 operations with bus traffic from other Teledyne LeCroy analyzers including USB, PCI Express, SAS or SATA.

### Identify and Capture Failures

The Kibra 480 Compliance Analyzer will identify any test failure and in addition has the ability to automatically capture bus traffic around the failure to assist in quickly identifying and solving problems.



### Extensive Testing

The Kibra 480 Compliance Analyzer includes a comprehensive suite of tests to ensure compatibility of devices to JEDEC specifications.

Timing Violation	Comments
	[ACT] [Mirrored Address] CS1 BG0 BA2 Row : 0x0080
	[Timing Violation]
FAW	V04: Four ACT Window < tFAW (23 clocks) Violation occurred in Rank:1 Last First ACT command to here(ns) 0 000 000 016.235 ns Invalid ACT at 0.000 000 427 840 s First ACT command at 0.000 000 411 605 s ACT should have occurred after 0.000 000 433 570 s
	[ACT] [Mirrored Address] CS1 BG2 BA3 Row : 0x6b84
	[Timing Violation]
RRD-DBG	V47: ACT to ACT (different bank group, same rank) < tRRD-S (4 clocks) Violation occurred in Rank:1 Last ACT command to here(ns) 0 000 000 000.955 ns Invalid ACT at 0.000 000 428 795 s ACT command at 0.000 000 427 840 s ACT should have occurred after 0.000 000 431 660 s
	[Timing Violation]
FAW	V04: Four ACT Window < tFAW (23 clocks) Violation occurred in Rank:1 Last First ACT command to here(ns) 0 000 000 016.235 ns Invalid ACT at 0.000 000 428 795 s First ACT command at 0.000 000 412 560 s ACT should have occurred after 0.000 000 434 525 s
	[DES]
	[ACT] [Mirrored Address] CS1 BG2 BA0 Row : 0x0100
	[Timing Violation]
RRD-SBG	V03: ACT to ACT (same bank group) < tRRD-SBG (6 clocks) Violation occurred in Rank:1 Last ACT command to here(ns) 0 000 000 001.910 ns Invalid ACT at 0.000 000 430 705 s ACT command at 0.000 000 428 795 s ACT should have occurred after 0.000 000 434 525 s
	[Timing Violation]
RRD-DBG	V47: ACT to ACT (different bank group, same rank) < tRRD-S (4 clocks) Violation occurred in Rank:1 Last ACT command to here(ns) 0 000 000 002.865 ns Invalid ACT at 0.000 000 430 705 s ACT command at 0.000 000 427 840 s ACT should have occurred after 0.000 000 431 660 s
	[Timing Violation]



## Specifications

### Analyzer System Specifications

Host Machine Minimum Requirements	Microsoft® Windows® 8, Windows 7, Windows XP, Windows Server 2012, Windows Server 2008R2; 2 GB of RAM; Storage with at least 200 MB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; USB 2.0 port and/or 100/1000 Mbps Ethernet network interface. For optimal performance, please refer to our recommended configuration in the product documentation.
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Protocols Supported	DDR3 and DDR4
Recording Memory Size	4 GB
Data Rates Supported	DDR3: 400 MHz to 1066 MHz DIMM clock speeds DDR4: 800 MHz to 1200 MHz DIMM clock speeds
Probe Interface	DDR3 & DDR4 UDIMM, RDIMM, SODIMM slot interposers
DIMM Compatibility	Compatible with all standard 240-pin DDR4 SRAM DIMMs up to 2400 MT/s
Analysis Capability	Analysis is performed on up to 4 ranks using channel 1 slot; up to 8 ranks when using both channel 1 and channel 2
Front Panel LEDs	Power, Status, Trigger
Front Panel Connectors	Cable Interface to DIMM Slot 1 Interposer; Cable Interface to DIMM Slot 2 Interposer; External RefClk-IN (SMA); External Read/Write Trigger Output (SMA); Interposer Probe Power Connector
Rear Panel Connectors	CrossSync Connector; USB 2.0 Connection to host machine; Trigger IN (SMA); Trigger OUT (SMA)
Dimensions (W x H x D)	20 x 3.2 x 23 cm (8" x 1.25" x 9")
Analyzer to DUT Cable	457 mm (18")
Weight	1.5 Kg (3.4 lbs)
Power Requirements	External 12V DC Power (from supplied adapter)
Environmental Requirements	Operating: 0 to 55C (32 to 131F) Non-operating: -20 to 80C (-4 to 176F) Humidity: 10 to 90% RH (non-condensing)



Rear Panel of Kibra 480

## Ordering Information

### Product Description

### Product Code

#### Models

Kibra 480 DDR3 Compliance Analyzer	DDR-CS03-D02-X
Kibra 480 DDR4 Compliance Analyzer	DDR-CS04-D02-X

#### Kibra 480 Options for DDR4

Kibra 480 DDR4 DIMM Slot 1 Interposer	DDR-AC22-D02-X
Kibra 480 DDR4 DIMM Slot 2 Interposer	DDR-AC23-D02-X
Kibra 480 DDR4 Analysis Upgrade License Key	DDR-AC09-D02-A
Kibra 480 DDR4 SODIMM Slot 1 Interposer	DDR-AC24-D02-X
Kibra 480 DDR4 SODIMM Slot 2 Interposer	DDR-AC25-D02-X

#### Kibra 480 Options for DDR3

Kibra 480 DDR3 DIMM Slot 1 Interposer	DDR-AC10-D02-X
Kibra 480 DDR3 DIMM Slot 2 Interposer	DDR-AC11-D02-X
Kibra 480 DDR3 SODIMM Slot 1 Interposer	DDR-AC16-D02-X
Kibra 480 DDR3 SODIMM Slot 2 Interposer	DDR-AC17-D02-X

#### Kibra 480 Advanced Features

Advanced Analysis	DDR-AF01-D02-A
Advanced Triggering	DDR-AF02-D02-A
Memory Mapping	DDR-AF03-D02-A
Follow MRS	DDR-AF04-D02-A
Performance Analysis	DDR-AF05-D02-A
Advanced Reports	DDR-AF06-D02-A
Advanced Searching	DDR-AF07-D02-A

#### Accessories

Mounting Bracket Kit	ACC-BRKT-013-X
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